4. (Previously Presented) Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse.

5. (Previously Presented) Capacitive voltage multiplier according to claim 4, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors.

6. (Previously Presented) Capacitive voltage multiplier according to claim 4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level.

7. (Previously Presented) Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used.

8. (Original) Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage.

REMARKS

Claims 1-8 are pending. In the outstanding Office Action, the Examiner rejected claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Kazerounian et al.,

U.S. Patent No. 5,086,974, in view of Yu, U.S. Patent No. 6,304,007. Applicant respectfully traverses these rejections.

Independent claim 1 is directed to a capacitive voltage multiplier for generating voltage pulses. The multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier. The switching capacitor circuit (21) is provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse. The multiplier is characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier. The diode chain circuit (22) comprises a diode-chain and pumping capacitors for delivering high voltage current.

The Examiner asserts that circuit element 103 (see FIG. 2 of Kazerounian; also note that "103" in FIG. 2 points to both a circuit element and to capacitors) in Kazerounian is the "diode chain circuit" in independent claim 1. The Examiner asserts that it would be obvious to combine the text at col. 1, lines 18-22 in Yu (which the Examiner equates with a "switching capacitor circuit" in independent claim 1) with the "diode chain circuit" (e.g., 103) in Kazerounian. Kazerounian states the following:

> Switching capacitor is one of the original concepts for the energy conversion. It is available in very limited application such as the energy source for high voltage discharge by connecting an array of capacitors in parallel configuration for charging and in series configuration for discharging.

Kazerounian, col. 1, lines 18-22. It is also noted that the circuit in FIG. 2 of Yu appears to be a circuit that charges capacitors in parallel and discharges the capacitors in series and that produces an output voltage that is higher than the input voltage.

It is respectfully submitted that the combination of Kazerounian and Yu is improper. Specifically, there is no motivation to combine Kazerounian and Yu and Kazerounian.

Before proceeding further with this argument, it is helpful to review Kazerounian. Kazerounian states the following:

> In accordance with one novel feature of our invention, a voltage regulator circuit 108 is coupled to output lead 104 to ensure that voltage V_{OUT} is at a desired value which is independent of temperature and process parameters. Voltage regulator 108 includes capacitors 110-1 to 110-4 coupled in series between output lead 104 and a ground terminal 112. Capacitors 110-1 to 110-4 all have a substantially identical capacitance, and serve as a capacitive voltage divider so that the voltage at a node 114 (between capacitors 110-3 and 110-4) is at a voltage equal to voltage $V_{OUT}/4$. Node 114 is connected to the non-inverting input lead of a comparator 116. The inverting input lead of comparator 116 is connected to a lead 118 which receives a reference voltage V_{REF}. Comparator 116 compares voltage V_{OUT} with voltage V_{REF} and generates a binary output signal on an output lead 119 in response thereto. Lead 119 is connected to a NAND gate which is part of ring oscillator circuit 124. When the signal at lead 119 is high, ring oscillator 124 oscillates and provides output signals ϕ and $\overline{\phi}$ to the voltage multiplier. Thus, if the signal at lead 114 is less than voltage V_{REF}, ring oscillator 124 generates clock signals ϕ and $\overline{\phi}$, and thus voltage multiplier 100 will increase voltage V_{OUT} at lead 104. However, as soon as voltage $V_{OUT}/4$ is greater than voltage V_{REF}, the signal at output lead 119 goes low, ring oscillator 124 stops oscillating and voltage multiplier 100 stops increasing voltage V_{OUT}. Thus, the EEPROM of the present invention includes a voltage regulator which permits voltage V_{OUT} to be accurately controlled.

Kazerounian, col. 8, lines 9-38.

Furthermore, the circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** Vout 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. In particular, Kazerounian states the following:

> This process continues until a voltage is selected which is sufficient for erasing the EEPROM. Thereafter, the contents of nonvolatile register 106 are no longer changed, and the EEPROM is erased with the selected voltage. By limiting voltage V_{OUT} to a voltage large enough to erase the EEPROM but not greater, the transistors exposed to voltage V_{OUT} will not be excessively stressed.

Kazerounian, col. 9, lines 31-38.

Based on the cited sections of Kazerounian, Applicant reads Kazerounian as providing a voltage multiplier circuit 100 that allows selection of a reference voltage, V_{REF}, based on contents of a register. A comparator 116 compares V_{REF} with another voltage that is equivalent to $V_{OUT}/4$ because of the voltage divider of the capacitors 110-1 through 110-4. When V_{REF} is less than $V_{OUT}/4$, the comparator causes the ring oscillator circuit 124 (incorrectly marked as "123" in FIG. 2 of Kazerounian) in Kazerounian to oscillate and produce the signals ϕ and $\overline{\phi}$, which are input to the element 103 and cause V_{OUT} to rise. Once V_{REF} is approximately equivalent to $V_{OUT}/4$, the comparator stops oscillation of the ring oscillator circuit 124 in Kazerounian and V_{OUT} ceases to rise. Using a particular process, the lowest V_{OUT} is selected that will allow the EEPROM to be erased.

Therefore, Kazerounian discloses a voltage multiplier circuit 100 that is carefully designed to allow selection of the lowest V_{OUT} that will allow the EEPROM to be erased. Into this carefully designed system, the Examiner adds another voltage multiplier as purportedly described in Yu, "in order to provide a simple way of multiplying, pump or step up the voltage of the capacitive array that is one of the earliest and original concept of energy conversion for boosting/multiplying power." Applicant respectfully disagrees.

One court discussed an obviousness rejection under §103 as follows. "In making the assessment of differences [i.e., between the prior art and the claimed invention], section 103 specifically requires consideration of the claimed invention 'as a whole.'" Ruiz v. A.B. Chance Co., 69 USPQ2d 1686, 1690 (Fed. Cir. 2004). In Ruiz, the court also stated the following:

> This court has provided further assurance of an "as a whole" assessment of the invention under §103 by requiring a showing that an artisan of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would select the various elements from the prior art and combine them in the claimed manner. In other words, the examiner or court must show some suggestion or motivation, before the invention itself, to make the new combination.

Id., citing In re Rouffet, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998). For at least the following reasons, Applicant respectfully submits that there is no suggestion or motivation for one skilled in the art to make the combination of Kazerounian and Yu as suggested by the Examiner.

First, the circuitry of Kazerounian already produces a high output voltage on Vout 104 (see FIG. 2 of Kazerounian). There is no benefit to adding yet another circuit (i.e., from Yu) for producing a high voltage on Vout 104 of Kazerounian.

Second, combining two circuits (element 103 in Kazerounian and the circuit described at col. 1, lines 18-22 of Yu), each of which produces a high voltage from a lower input voltage, would appear to provide no benefits and many detriments. The circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** Vout 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. Adding another circuit that produces an even higher voltage at Vout 104 would be counterproductive and may render impossible the careful selection of Vout 104. For instance, Vout 104 in such a combined system would now depend on two circuits for producing a high voltage output instead of basically a single circuit (element 103) in Kazerounian. Furthermore, the Yu circuit does not appear to have an adjustable voltage and does not appear to be able to be controlled by elements (e.g., capacitors 110, the ring oscillator circuit 124, the circuits adjusting V_{REF}, and the comparator 116) in Kazerounian that select a voltage on Vout 104. Therefore, the combination of Kazerounian and Yu may not provide adjustable V_{OUT}, which is one of the reasons Kazerounian was invented.

Finally, Kazerounian teaches away from a combination of Kazerounian and Yu. As one example, Kazerounian states that one problem being overcome is the following:

> It is also known in the art to provide circuits for regulating the output voltage provided by voltage multipliers. Unfortunately, such regulating circuits typically control the voltage multiplier output voltage to a value dependent on manufacturing process parameters and temperature. Thus, the erase voltage can vary from production lot to production lot, and can also vary

> in response to ambient temperature. Thus, despite the presence of the regulator circuit, ***the output voltage might be*** either ***too high (in which case it might stress or damage the transistors in the EEPROM circuit)*** or too low (in which case it will not erase the EEPROM).

Kazerounian, col. 2, lines 8-19 (emphasis added). Kazerounian further states the following:

> The reference voltage is typically set to a value by voltage trimming circuitry such that the voltage multiplier output voltage is sufficiently high to erase the EEPROM but not significantly higher. Thus, the erase voltage is not permitted to vary, and become so high as to stress or damage transistors in the EEPROM, or become so low as to prevent erasure of the EEPROM.

Kazerounian, col. 3, lines 18-25. Kazerounian apparently fixes a problem of having too high an output voltage. Thus, Kazerounian teaches against higher output voltages (V_{OUT}) and is designed to allow selection of a ***lower*** output voltage. By contrast, a combination of Kazerounian with Yu would ***increase*** the output voltage, which means that Kazerounian teaches away from a combination of Kazerounian and Yu.

As another example, Kazerounian is also directed to producing a V_{OUT} that is independent of manufacturing process parameters and temperature. See Kazerounian at col. 2, lines 8-19 and col. 2, line 67 to col. 3, line 2. Kazerounian also states the following:

> The above-described voltage regulator provides a number of important advantages. First, as can be seen in equations 1 to 3, voltage V_{REF} is independent of capacitance C. Thus, if capacitors 120-1 to 120-20, 122-1 to 122-10 or 124-1 to 124-10 are made either too large or too small (e.g. because of underetching or overetching the polysilicon capacitor plates during manufacturing), voltage V_{REF} does not change. Thus, voltage V_{REF} is insensitive to processing conditions. More importantly, voltage V_{REF} is insensitive to temperature.

Kazerounian, col. 9, lines 39-48. Further, the circuit 100 of Kazerounian appears specifically designed so that the output voltage of element 103 in Kazerounian does not involve creating an output voltage by using a set of capacitors. In fact, because in Kazerounian a comparison of V_{REF} with V_{OUT} is used to adjust V_{OUT}, the circuit 100 of Kazerounian is insensitive (as described in Kazerounian) to processing conditions and temperature effects.

If Yu, which the Examiner asserts describes a voltage multiplier using capacitors, is combined with Kazerounian, there would be capacitors that would be used to generate V_{OUT}. As stated in the cited text above from Kazerounian, capacitance in the capacitors is affected by processing conditions and/or temperature. Because the combination of Kazerounian and Yu would now have capacitors that help to generate V_{OUT}, then the combined system of Kazerounian and Yu would no longer be independent of manufacturing process parameters and temperature, as the capacitance of the capacitors is affected by processing conditions and/or temperature. Therefore, Kazerounian teaches away from a combination of Kazerounian and Yu, as Kazerounian teaches that insensitivity to processing conditions and temperature is desirable but a combination of Kazerounian and Yu would be sensitive to processing conditions and temperature.

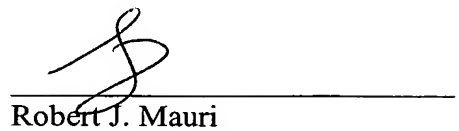
For at least these reasons, Kazerounian teaches away from combining Kazerounian and Yu.

It is respectfully submitted that the invented arrangement in claim 1 is not obvious and has so far never been disclosed by cited art. Further, it is certainly not at all obvious that a combination of the cited standard voltage multipliers in Kazerounian and Yu would provide results provided by the claimed invention of claim 1, e.g., fast output voltage changes yet with a long active state output voltage stability as well as charge conservation (e.g., energy preservation) when switching to the inactive state.

The placement of the diodes as shown in the block diagrams of the present invention and claimed by claim 1 is important and not obvious and cannot as such be found in the standard parallel connection of voltage multipliers of record.

Applicant respectfully requests the §103(a) rejection of claim 1 be withdrawn. Because independent claim 1 is patentable, its dependent claims 2-8 are patentable for at least the reasons given with respect to claim 1.

Respectfully submitted:



5/31/06

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